REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed September 16, 2009. Through this response, claims 38, 53-55 and 78 have been amended, claims 66-70 have been canceled without prejudice, waiver, or disclaimer, and claim 89 has been added without the introduction of new matter. Reconsideration and allowance of the application and pending claims 38, 53-55, 71-78, 80-82, and 85-89 are respectfully requested.

I. Substance of Interview Pursuant to MPEP § 713.04

Applicants' representative, Dave Rodack (Reg. No. 47,034) requested and obtained a telephone interview with Examiner Shawn S. An. The interview was conducted on December 4th, 2009, commencing at 10:30AM eastern time, and focused on the rejections levied in the non-final Office Action dated September 16th, 2009, and in particular, the rejections under 35 U.S.C. § 101, 112, and 103 for the respective independent claims 38, 53, 54, 55, and 66. With regard to the rejections under 35 U.S.C. § 101 and 112, Examiner An explained his position on those rejections, and Applicants' representative and Examiner An discussed various options with regard to those rejections. With regard to the 35 U.S.C. § 103 rejection, the manner of operation pertaining to resolution processing in references *MacInnis* (U.S. Patent No. 6,570,579), *Boyce* (U.S. Patent No. 5,614,952), and *Kalra* (5,953,506) was discussed, as was the manner of downscaling in relation to a memory component described in Applicant's disclosure and one or more of the claims. Mr. Rodack expressed appreciation for the opportunity to discuss the rejection, and no exhibits were presented and no agreements were reached. Applicants' representative acknowledges the Interview Summary dated December 8, 2009.

II. Claim Rejections – 35 U.S.C. § 101

Claims 66-70 have been rejected under 35 U.S.C. §101 because the preamble of the claims is allegedly directed to non-statutory subject matter. In an effort to advance prosecution of the claims and facilitate allowance, Applicants have canceled claims 66-70 without prejudice, waiver, or disclaimer. Accordingly, Applicants respectfully submit that the rejection has been rendered moot and respectfully request that the rejection be withdrawn.

III. Claim Rejections - 35 U.S.C. § 112(1)

Claims 54, 78, 80-81, and 87 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. Applicants have amended claims 54 and 78 consistent with FIGs. 2 and 4 of Applicants' application as filed, as well as consistent with page 12, lines 3-16 and FIG. 5 and the accompanying description. It is respectfully submitted that the components of the media engine described at least in part in claim 54 comprise a circuit (e.g., ASIC) that cooperates with the processor and the media engine, and hence are fully supported by the specification as filed and do not introduce new matter. For at least these reasons, Applicants respectfully request that the rejection be withdrawn as the amendments have rendered the rejection moot.

IV. Claim Rejections - 35 U.S.C. § 103(a)

A. Statement of the Rejection

Claims 38, 53-55, 66-78, 80-82, and 85-88 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 6,570,579 to *MacInnis et al.* ("*MacInnis*") in view of U.S. Patent No. 5,614,952 to *Boyce et al.* ("*Boyce*") and U.S.

Patent No. 5,953,506 to *Kalra et al.* ("*Kalra*"). Applicants respectfully traverse this rejection to the extent not rendered moot by amendment.

B. Discussion of the Rejection

The U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP 2100-116, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

Applicants respectfully submit that a *prima facie* case of obviousness is not established using the art of record. Applicants have made some minor and/or clarifying amendments consistent with the discussion in the Examiner Interview, such as removing the "providing" element and incorporating the capability of the DHCT operating in different modes with the determination elements (claims 38 and 53), or replacing the "providing" element with "operating" (claim 55). Claim 54 removes the "determining" element and removes "logic" in favor of various components as described above. In addition, Applicants have amended claims 38 and 55 to clarify, consistent with other independent claims (e.g., claims 53 and 54), that the video picture is downsampled post-capture in the memory component (i.e., the first portion of the memory component), hence addressing the possibility discussed in the Examiner Interview that some of the claims may not specifically tie these features together.

Independent Claim 38

Claim 38 recite (with emphasis added):

> 38. A method for adapting to resource constraints of a digital home communication terminal (DHCT), said method comprising steps of:
> determining by the DHCT whether one of a resource-constrained mode or a non-resource constrained mode is to be initiated, the DHCT capable of operating in the non-resource constrained mode and a plurality of resource constrained modes;
> responsive to determining that one of the resource-constrained modes is to be initiated, operating the DHCT in the determined resource-constrained mode, including:
> ***retrieving a set of reconstructed decompressed video frames from a first portion of a memory component, wherein the memory component stores compressed video frames in a distinct second portion, wherein the set of video frames corresponds to a video picture stored in the first portion***; and
> ***transferring the set of retrieved reconstructed decompressed video frames to a display device while downscaling the video picture in transit to the display device.***

Applicants respectfully submit that claim 38 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra*. Briefly, claim 38 as amended comprises elements that are arranged to cover at least one embodiment where a compressed picture buffer and decoded picture buffer reside in media memory, and downscaling is implemented on the video picture in transit between the decoded picture buffer and the display device. In contrast, Applicants respectfully submit that the cited art of record operates in a fundamentally different manner.

For instance, with regard to *MacInnis*, the non-final Office Action (page 4) acknowledges that *MacInnis* does not show the 2-component memory, nor does *MacInnis* disclose or teach the in-transit downscaling features of claim 38. Though *MacInnis* appears to focus attention on primarily graphics processing, *MacInnis* describes video decoding and capture and scaling at least in association with Figure 5 (reproduced below).

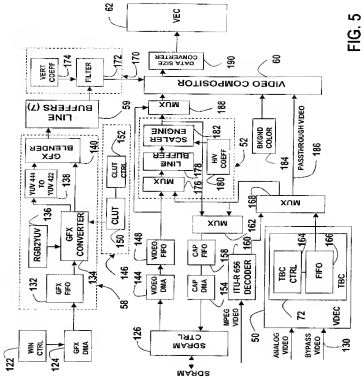


FIG. 5

In particular, col. 11, lines 39 – col. 12, line 7 of *MacInnis* provides as follows (emphasis added):

> Analog video or MPEG video may be provided to the video compositor as passthrough video. Alternatively, either type of video may be captured into memory and provided to the video compositor as a scaled video window. The digitized analog video signals preferably have a pixel sample rate of 13.5 MHz, contain a 16 bit data stream in YUV 4:2:2 format, and include timing signals such as top field and vertical sync signals.
>
> The VDEC 50 includes a time base corrector (TBC) 72 comprising a TBC controller 164 and a FIFO 166. To provide passthrough video that is synchronized to a display clock preferably without using a frame buffer, the digitized analog video is corrected in the time domain in the TBC 72 before being blended with other graphics and video sources. During time base correction, the video input which runs nominally at 13.5 MHZ is

> synchronized with the display clock which runs nominally at 13.5 MHZ at the output; these two frequencies that are both nominally 13.5 MHz are not necessarily exactly the same frequency. In the TBC, the video output is preferably offset from the video input by a half scan line per field.
>
> A capture FIFO 158 and a capture DMA 154 preferably capture the digitized analog video signals and MPEG video. The SDRAM controller 126 provides captured video frames to the external SDRAM. A video DMA 144 transfers the captured video frames to a video FIFO 148 from the external SDRAM.
>
> The digitized analog video signals and MPEG video are preferably scaled down to less than 100% prior to being captured and are scaled up to more than 100% after being captured. The video scaler 52 is shared by both upscale and downscale operations. The video scaler preferably includes a multiplexer 176, a set of line buffers 178, a horizontal and vertical coefficient memory 180 and a scaler engine 182. The scaler engine 182 preferably includes a set of two polyphase filters, one for each of horizontal and vertical dimensions.

In other words, it is clear that any alleged "downscaling" occurs prior to capture, not post-capture as described in association with claim 38. Such operation is consistent with *MacInnis*' expressed benefit (see Summary) of conserving memory.

Likewise, *Kalra*, though apparently used for alleged teaching of the various mode operations as described in claim 38, appears to scale the video in the network (by sending a base and additive streams based on a profile provided by the client (see Summary, e.g., col. 2, lines 27-49, *Kalra*), addressing the presence of clients of differing capabilities in a network (see Background, e.g., col. 1, lines 21-58, *Kalra*). In other words, any reduction of resolution via scaling occurs pre-capture, not post-capture as claimed.

With regard to *Boyce*, the non-final Office Action (page 5) alleges the following (emphasis in original):

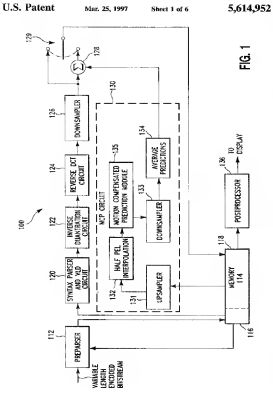
> Furthermore, Boyce et al teaches digital video decoder comprising retrieving a set of reconstructed decompressed (decoded) video data from a first portion (Fig. 1, 118) of a memory component (114), wherein the memory component stored compressed video data in a distinct second portion (116), wherein the set of video data corresponds to a video picture (col. 4, lines 64-67; col. 5, lines 1-4; col. 10, lines 44-50) for

> efficiently managing the memory resources such as size or the bandwidth (col. 10, lines 1-4).
>
> Moreover, Boyce et al teaches transferring the set of retrieved reconstructed decompressed (decoded) video data (from Fig. 4, 402 and 403) to a display device (TO DISPLAY) ***while*** downscaling (Reduced Resolution) the video picture in transit to the display device for implementing picture-in-picture capabilities in a digital TV without incurring the cost of multiple full resolution decoders (Fig. 4, col. 17, lines 66-67; col. 18, lines 1-16; col. 2, lines 37-40).

Applicants respectfully submit that *Boyce*, like *MacInnis* and *Kalra*, fails to describe downscaling after the decompressed picture buffer. It is noteworthy that the reduced resolution decoders 402 and 403 of FIG. 4 are used in the non-final Office Action to support the alleged teachings of downscaling in transit. However, Applicants believe that *Boyce* teaches that the decoders 402 and 403 are based on the operations and architecture of the decoder circuit 100 shown, for instance in Figure 1 of *Boyce*. For instance, *Boyce* describes the decoders 402 and 403 as containing components of the decoder circuit 100 (reproduced below), such as the IDCT circuit 124 (col. 18, line 16, *Boyce*), the IQ circuit 122 (col. 18, line 28, *Boyce*), and preparser 112 (col. 18, lines 39-46, *Boyce*). Further, the decoders 402 and 403 are described in col. 18, lines 33-38 of *Boyce* as follows (emphasis added):

> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

In other words, the decoders 402 and 403 not only store frames in reduced resolution format (and hence do NOT teach downscaling after the decompressed picture buffer), but also appear to share the same architecture as the decoder circuit 100. Figure 1 of *Boyce* is reproduced below:



The following excerpts from *Boyce* (reproduced below) support Applicants' position that *Boyce* (like *Kalra* and *MacInnis*) operate in a fundamentally different manner than claimed (emphasis added):

> *Col. 4, lines 34-39*: The method of the present invention for decoding HD and SD pictures includes the steps of reducing the resolution of received HD pictures prior to decoding by using, e.g., a preparser unit and/or adaptive field/frame downsampling to reduce the complexity of later processing stages of the decoder.
>
> *Col. 5, lines 25-44*: Because the cost and complexity of a HDTV decoder is largely a function of the requirement that it process large amounts of data on a real time basis, it is possible to reduce the complexity and thus the cost of a HDTV compatible decoder by reducing the amount of data that needs to be processed. While using only a small portion of the video data received in an HDTV signal will result in reduced resolution and picture quality, by carefully selecting which HDTV data to process and the method by which it is processed, video image quality comparable to or better than SD television signals can be achieved. As will be discussed below, the preparser 112 serves to dynamically limit the amount of video

data supplied to the remaining elements of the decoder circuit 100 including the syntax parser and VLD circuit 120 thereby reducing the amount of data that must be processed by the subsequent circuit elements on a real time basis and the required complexity of those circuit elements. An additional benefit of the use of the preparser 112 is that it permits for the use of a smaller coded data buffer 116 than would otherwise be required.

Col. 9, line 61 – col. 10, line 5: The output of the IDCT circuit 124 is coupled to the input of the downsampler 126. The downsampler 126 is used to downsample the data corresponding to each picture prior to storage in the frame buffer 118. As a result of the downsampling operation, the amount of data required to represent a video frame is substantially reduced. For example if the downsampler 126 is implemented to remove half of the digital samples used to represent a picture, the amount of data that would have to be stored will be reduced by a factor of approximately two substantially reducing the amount of memory required to implement the frame buffer 118.

Col. 11, lines 39-46: In accordance with the present invention, the downsampled frames supplied by the frame buffer 118 to the MCP circuit 130 are upsampled, e.g., on-the-fly, interpolated and then downsampled prior to generating predictions based on the motion vectors. In this manner the motion vectors which were originally generated based on full resolution video frames are effectively applied to downsampled video frames.

These excerpts from *Boyce* reveal that downsampling does not occur post-capture in a decoded picture buffer, but rather, pre-capture. For at least these reasons, Applicants respectfully submit that claim 38 is allowable over *MacInnis* in view of *Boyce* and *Kalra* and respectfully request that the rejection be withdrawn.

Because independent claim 38 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 71-73 and 85 are allowable as a matter of law for at least the reason that the dependent claims 71-73 and 85 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Independent Claim 53

Claim 53 recites (with emphasis added):

> 53. A method for adapting to resource constraints of a digital communication terminal (DHCT), said method comprising steps of:
> determining by the DHCT whether one of a plurality of resource-constrained modes is to be initiated, the DHCT capable of operating in a non-resource constrained mode and the plurality of resource-constrained modes;
> responsive to determining that one of the resource-constrained modes is to be initiated, initiating the resource-constrained mode, including:
> retrieving, from a first portion of a memory component, a set of compressed frames;
> storing, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution;
> ***retrieving, from the second and distinct portion of the memory component, the set of decoded frames; and***
> ***transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution.***

Applicants respectfully submit that claim 53 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra* for at least the reasons set forth above in association with claim 38, and hence respectfully submit that the rejection be withdrawn. Because independent claim 53 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 74-77 and 86 are allowable as a matter of law.

Independent Claim 54

Claim 54 recites (with emphasis added):

54. A digital home communication terminal (DHCT) comprising:
a processor;
a circuit configured to operate in a non-resource constrained mode and a plurality of resource-constrained modes, the circuit, responsive to instantiation of operation in the resource-constrained mode, configured in cooperation with the processor to:
retrieve, from a first portion of a memory component, a set of compressed frames;
store, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution;
retrieve, from the memory component, the set of decoded frames; and
transfer the set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution.

Applicants respectfully submit that claim 54 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra* for at least the reasons set forth above in association with claim 38, and hence respectfully submit that the rejection be withdrawn. Because independent claim 54 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 78, 80-81, and 87 are allowable as a matter of law.

Independent Claim 55

Claim 55 recites (with emphasis added):

> 55. A method for adapting to resource constraints of a digital home communication terminal (DHCT), said method comprising steps of:
> operating the DHCT in either a non-resource constrained mode or one of a plurality of resource-constrained modes, the DHCT capable of operating in the non-resource constrained mode and the plurality of resource-constrained modes;
> receiving, in a memory component, ***video frames each comprising a complete picture***;
> determining whether one of the resource-constrained modes is to be initiated;
> responsive to determining that one of the resource-constrained modes is to be initiated, initiating the resource-constrained mode, including:
> ***retrieving the video frames from the memory component; and***
> ***transferring the retrieved video frames to a display device while downscaling the retrieved video frames in transit to the display device.***

Applicants respectfully submit that claim 55 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra* for at least the reasons set forth above in association with claim 38, and hence respectfully submit that the rejection be withdrawn. Because independent claim 55 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 82 and 88 are allowable as a matter of law.

V. Canceled Claims

As identified above, claims 66-70 have been canceled from the application through this response without prejudice, waiver, or disclaimer. Applicants reserve the right to present these canceled claims, or variants thereof, in continuing applications to be filed subsequently.

VI. New Claims

As identified above, claim 89 has been added into the application through this response. Applicants respectfully submit that claim 89 is patentable over *MacInnis* in view of *Boyce* and *Kalra* for at least the reason that *MacInnis* in view of *Boyce* and *Kalra* fails to disclose, teach, or suggest at least "retrieving, from the second and distinct portion of the memory component, the set of decoded frames; and transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution." Accordingly, Applicants respectfully request that claim 89 be held allowable.

CONCLUSION

Applicants respectfully submit that Applicants' pending claims are in condition for allowance. Any other statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. In addition, any and all findings of inherency are traversed as not having been shown to be necessarily present. Furthermore, any and all findings of well-known art and official notice, and similarly interpreted statements, should not be considered well known since the Office Action does not include specific factual findings predicated on sound technical and scientific reasoning to support such conclusions. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

By: /DavidRodack/
David Rodack, Reg. No. 47,034

Merchant & Gould
P.O. Box 2903
Minneapolis, Minnesota 55402-9946
Telephone: 404.954.5066